

MOS FIELD EFFECT TRANSISTOR 2SK3108

SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

DESCRIPTION

The 2SK3108 is N channel MOS FET device that features a low on-state resistance and excellent switching characteristics, and designed for high voltage applications such as DC/DC converter.

ORDERING INFORMATION

PART NUMBER	PACKAGE
2SK3108	Isolated TO-220

FEATURES

- Gate voltage rating ± 30 V
- Low on-state resistance
 $R_{DS(on)} = 0.4 \Omega$ MAX. ($V_{GS} = 10$ V, $I_D = 4.0$ A)
- Low input capacitance
 $C_{iss} = 400$ pF TYP. ($V_{DS} = 10$ V, $V_{GS} = 0$ V)
- Avalanche capability rated
- Built-in gate protection diode
- Isolated TO-220 package

ABSOLUTE MAXIMUM RATING ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0$ V)	V_{DSS}	200	V
Gate to Source Voltage ($V_{DS} = 0$ V)	V_{GSS}	± 30	V
Drain Current(DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 8.0	A
Drain Current(pulse) ^{Note1}	$I_{D(pulse)}$	± 24	A
Total Power Dissipation ($T_A = 25^\circ\text{C}$)	P_{T1}	2.0	W
Total Power Dissipation ($T_C = 25^\circ\text{C}$)	P_{T2}	25	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note2}	I_{AS}	8.0	A
Single Avalanche Energy ^{Note2}	E_{AS}	51	mJ

Note1. $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

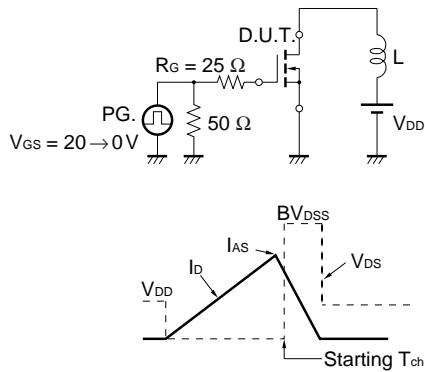
2. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 100$ V, $R_G = 25 \Omega$, $V_{GS} = 20$ V \rightarrow 0 V

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 Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

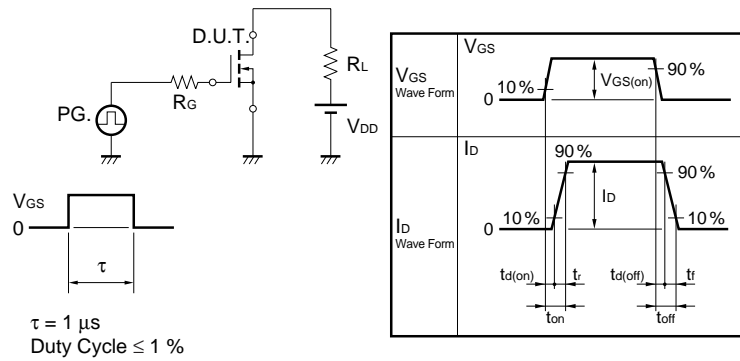
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain Leakage Current	I _{DSS}	V _{DS} = 200 V, V _{GS} = 0 V			100	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±30 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	2.5		4.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	1.5			S
Drain to Source On-state Resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 4.0 A		0.32	0.4	Ω
Input Capacitance	C _{iss}	V _{DS} = 10 V		400		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		110		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		55		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 100 V, I _D = 4.0 A		12		ns
Rise Time	t _r	V _{GS(on)} = 10 V		25		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		40		ns
Fall Time	t _f			20		ns
★ Total Gate Charge	Q _G	V _{DD} = 160 V		18		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		3.5		nC
Gate to Drain Charge	Q _{GD}	I _D = 8.0 A		10		nC
Diode Forward Voltage	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0 V		1.0		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0 V		250		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 50 A/μs		1.0		μC

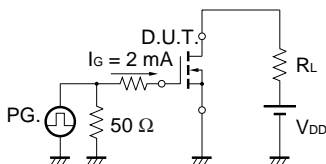
TEST CIRCUIT 1 AVALANCHE CAPABILITY



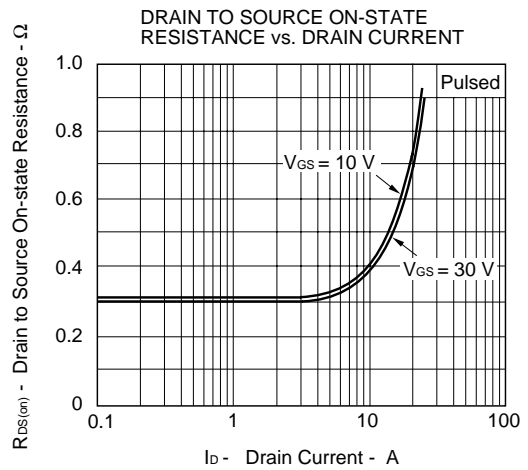
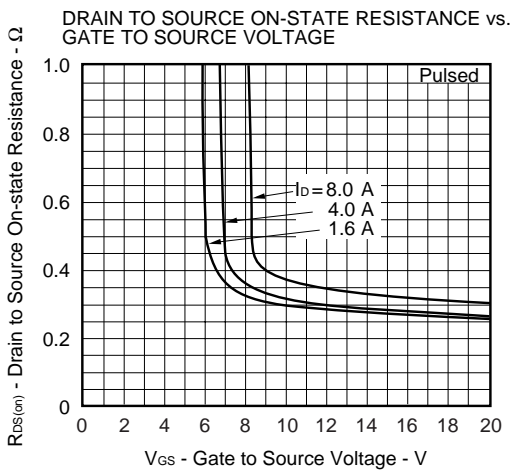
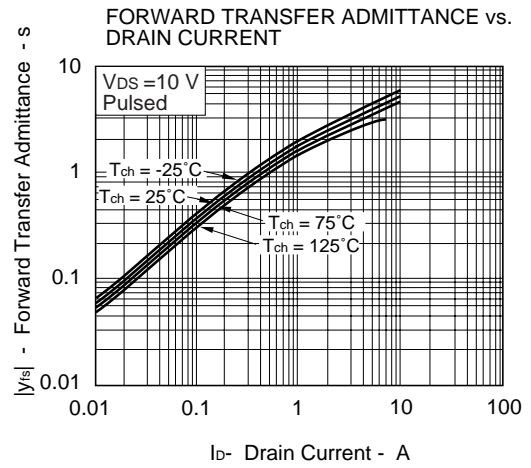
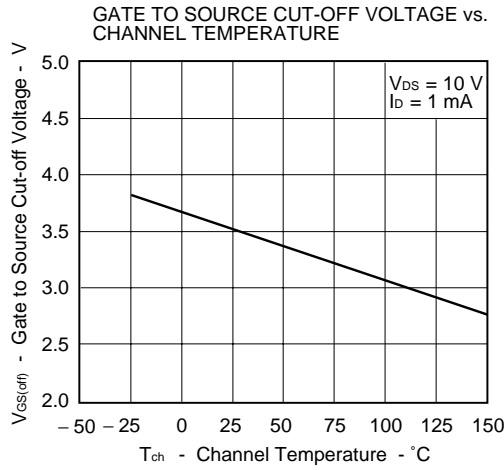
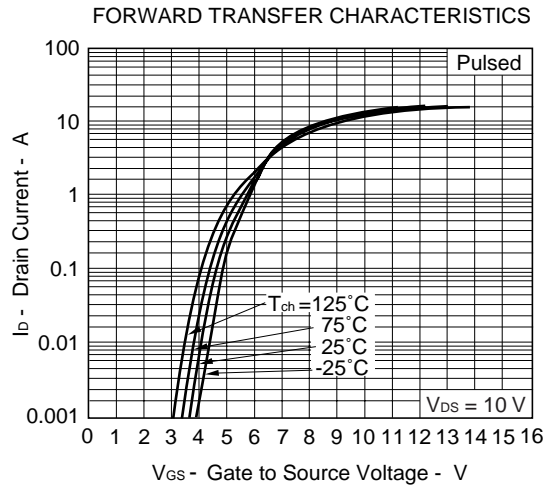
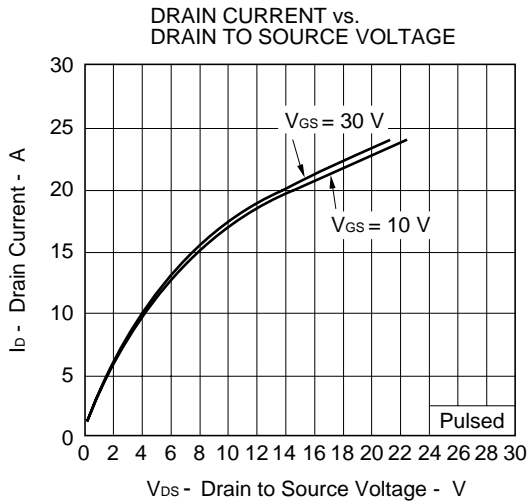
TEST CIRCUIT 2 SWITCHING TIME

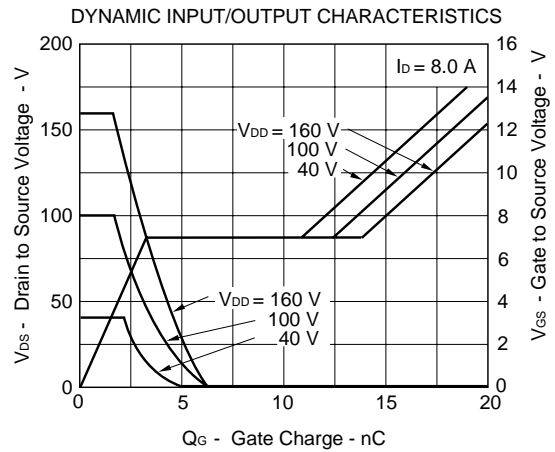
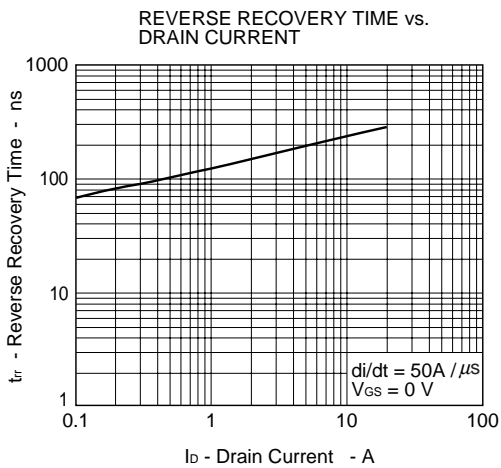
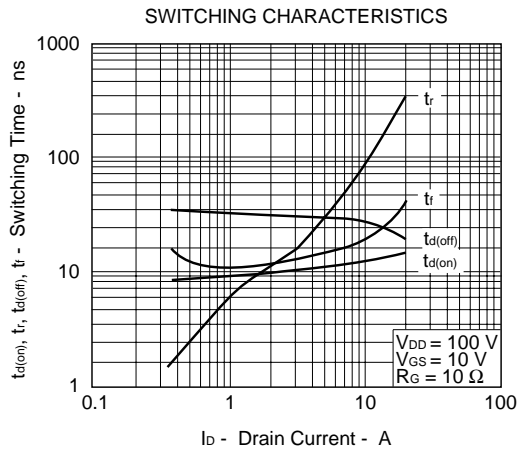
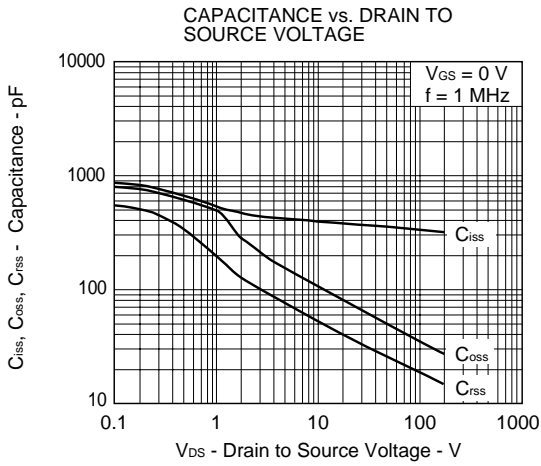
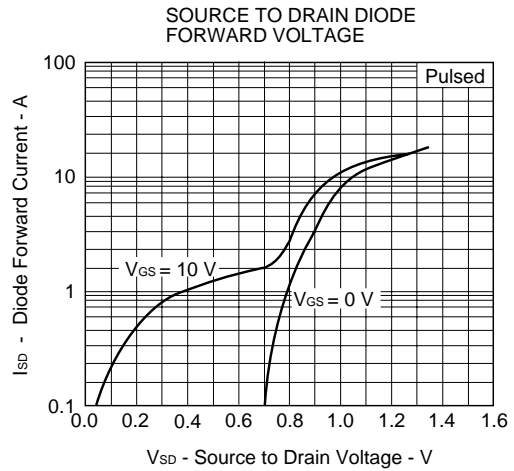
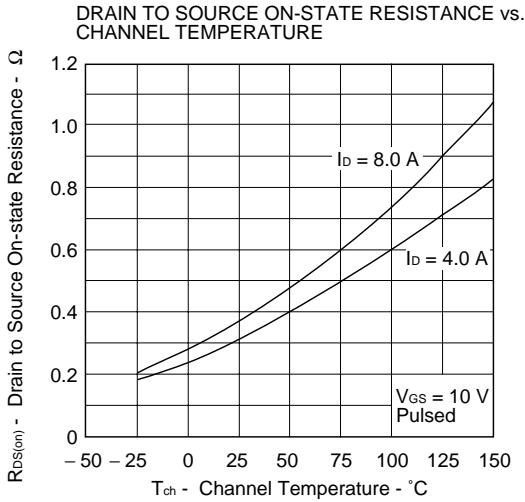


TEST CIRCUIT 3 GATE CHARGE

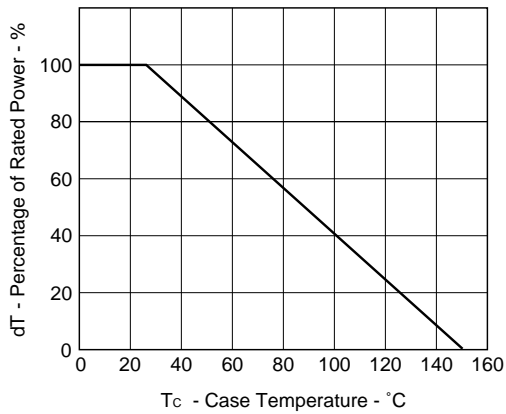


★ TYPICAL CHARACTERISTICS (T_A = 25°C)

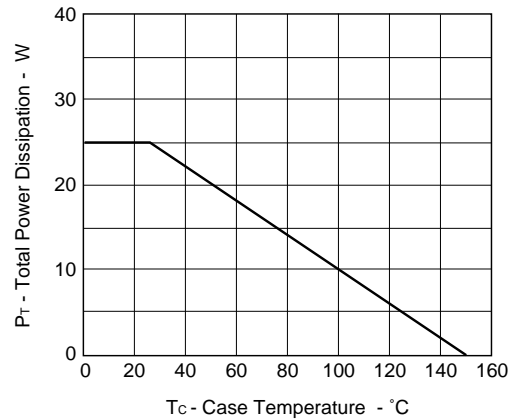




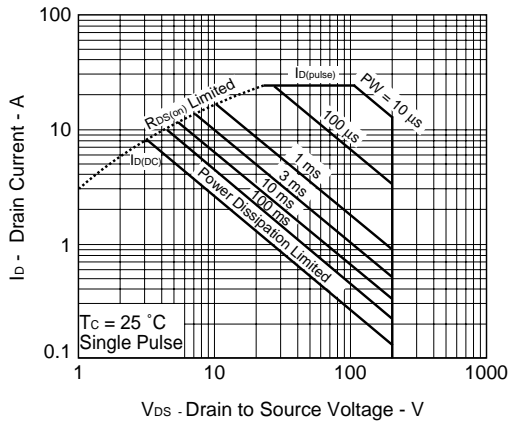
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



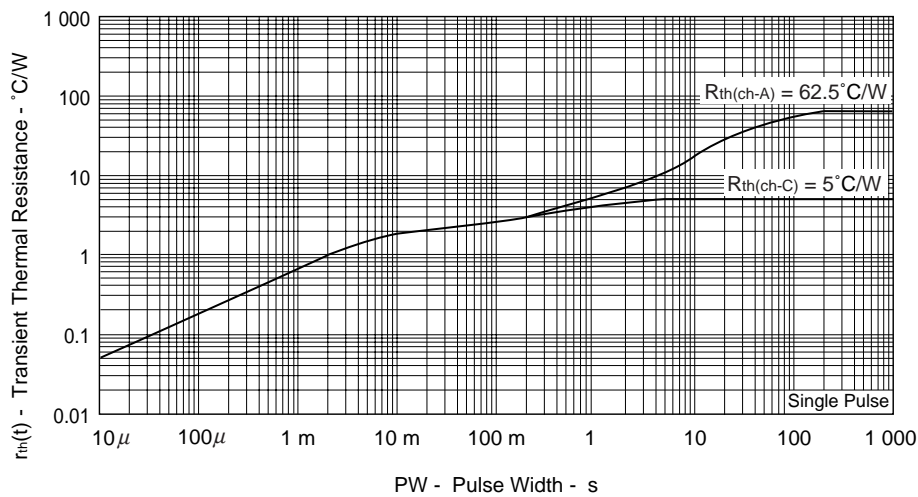
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

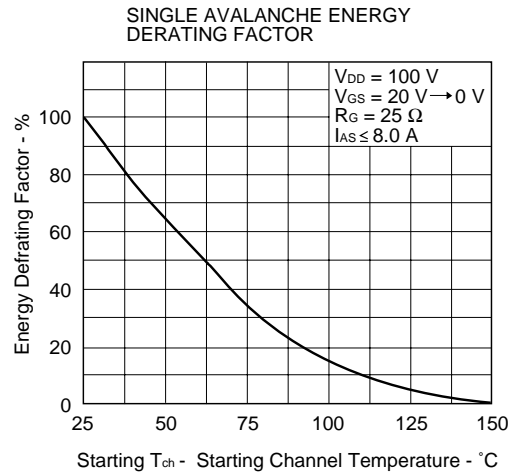
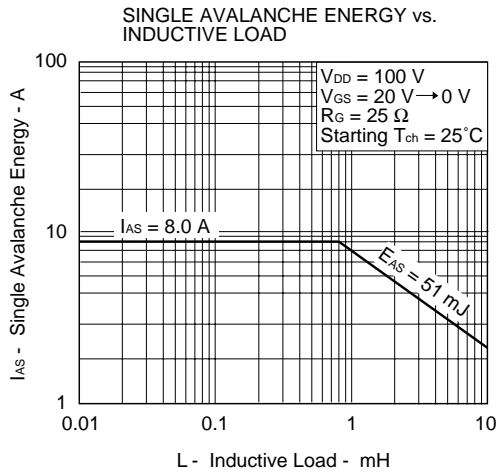


FORWARD BIAS SAFE OPERATING AREA



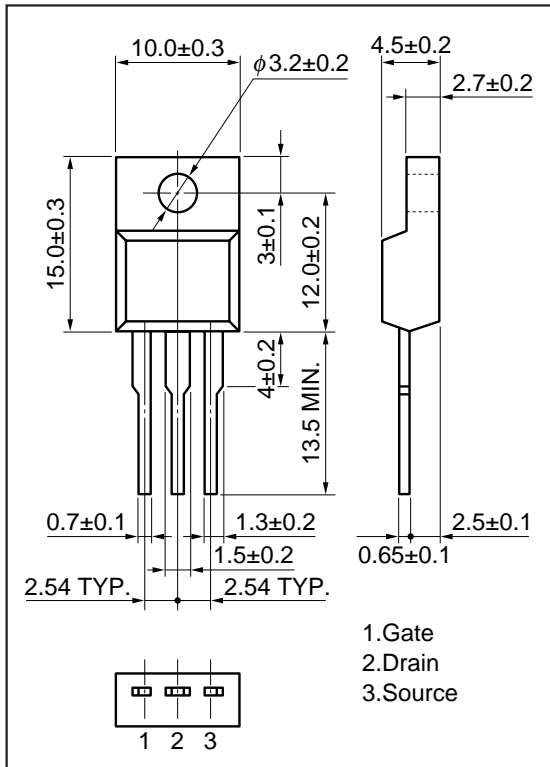
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



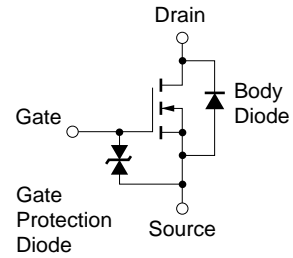


PACKAGE DRAWING(Unit : mm)

Isolated TO-220 (MP-45F)



EQUIVALENT CIRCUIT



The diode connected between the gate and source of the transistor serves as a protector against ESD.

When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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